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# A VLSI Processor for Fast Track Finding Based on Content Addressable Memories

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for the AMCHIP group:

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# Outline

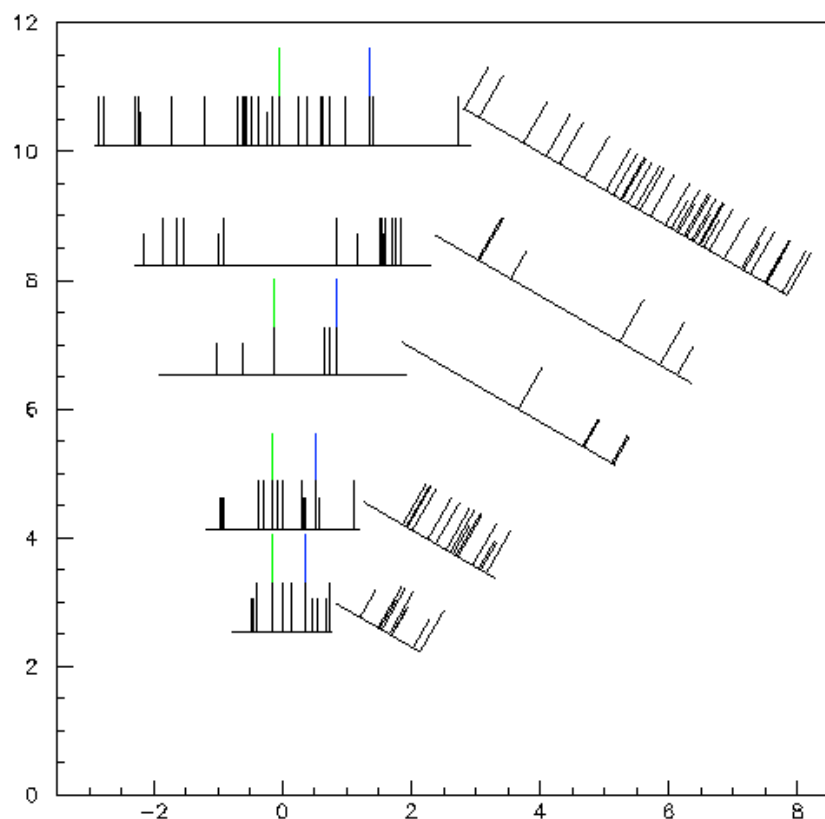
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- Motivations
- Working principle
- Design
- Features & performances
- Applications
- Production & tests
- Conclusions

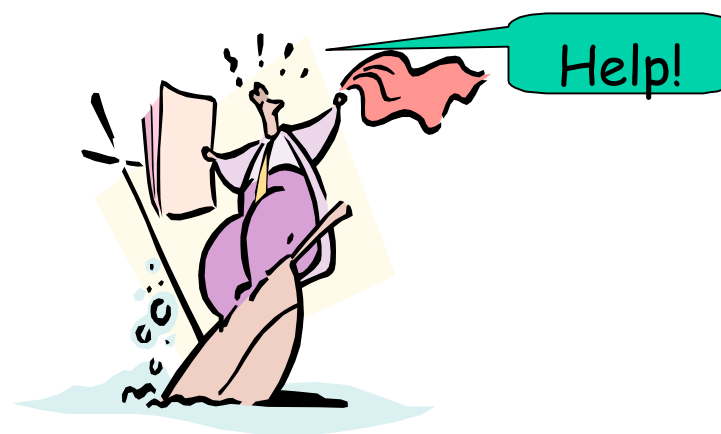
Hope to **share**  
this **technology**  
for **other**  
**experiments**

# The Tracking Problem

**CDF SVX:** would you recognize the yellow & blue tracks without colors?? **CMS 30 min. bias events** +  $H \rightarrow ZZ \rightarrow 4\mu$

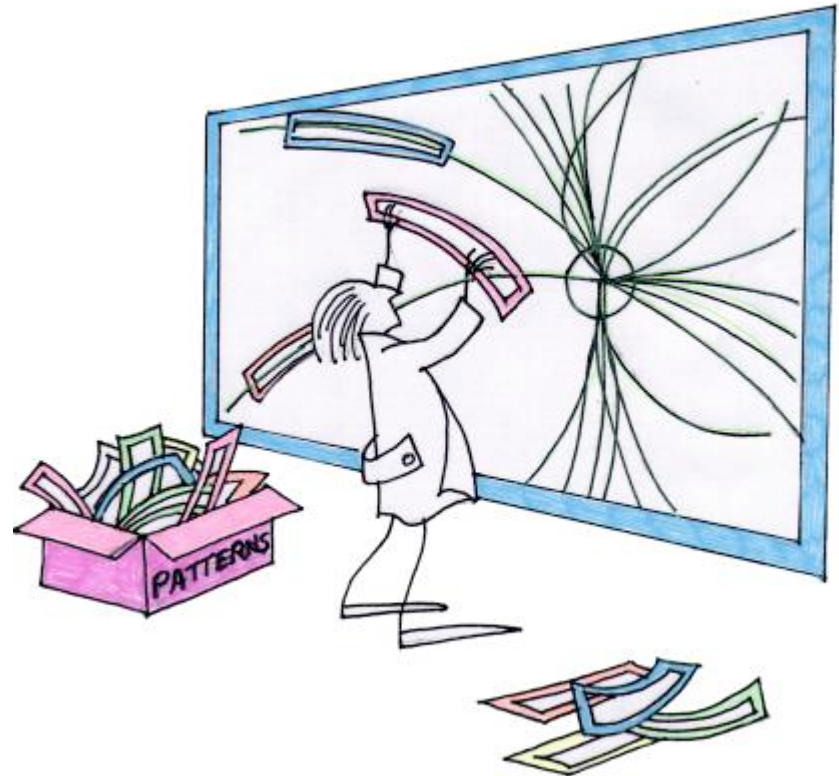
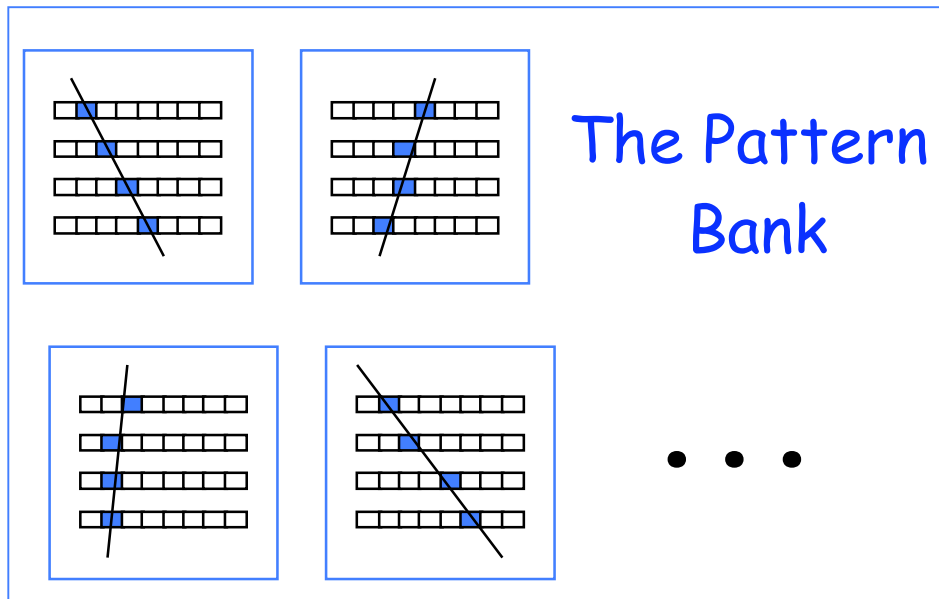
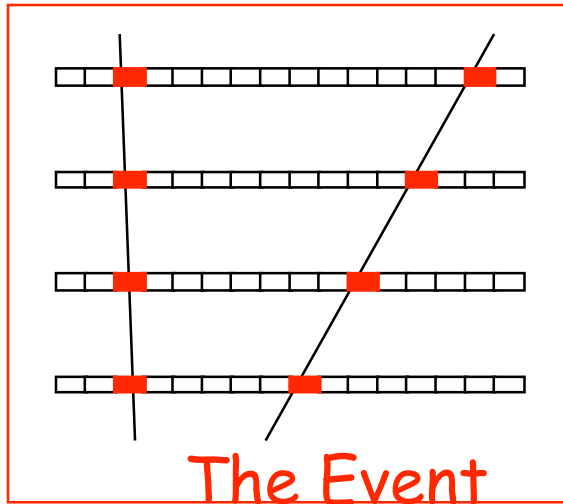


Where is the Higgs?



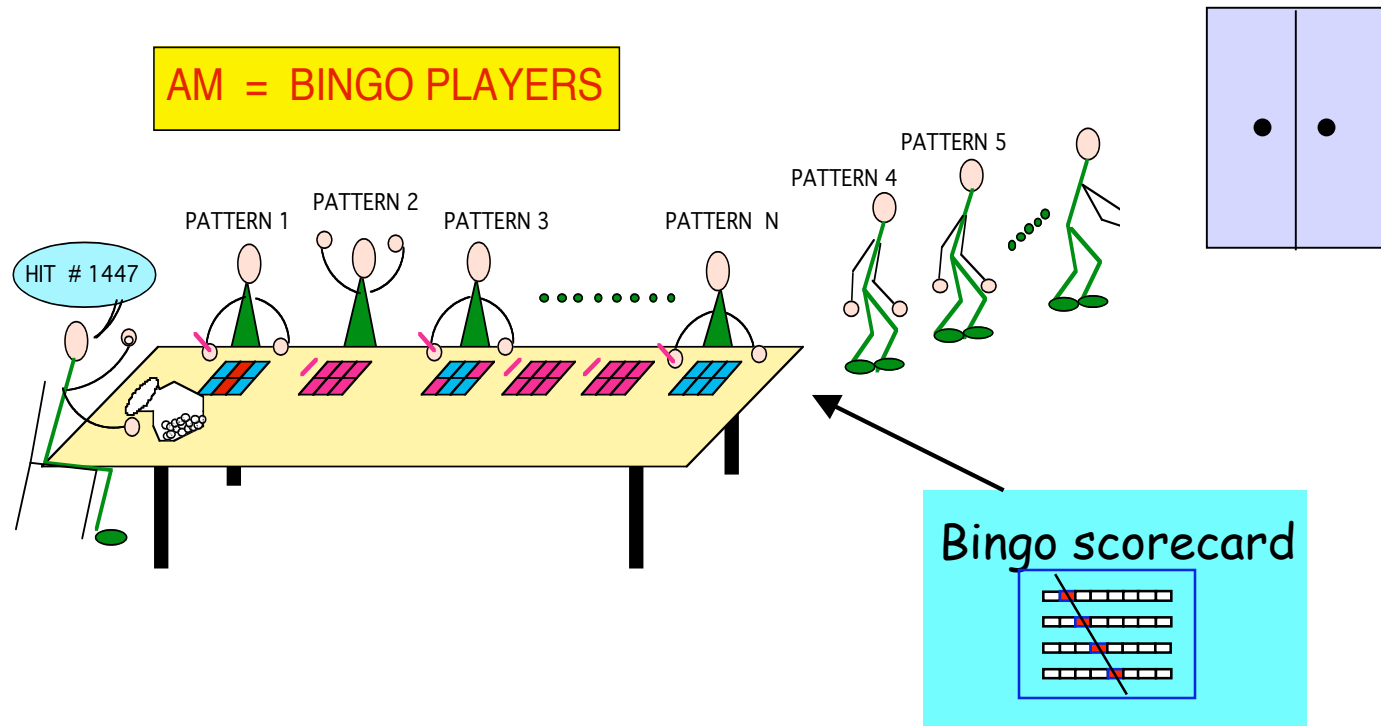
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# Pattern matching





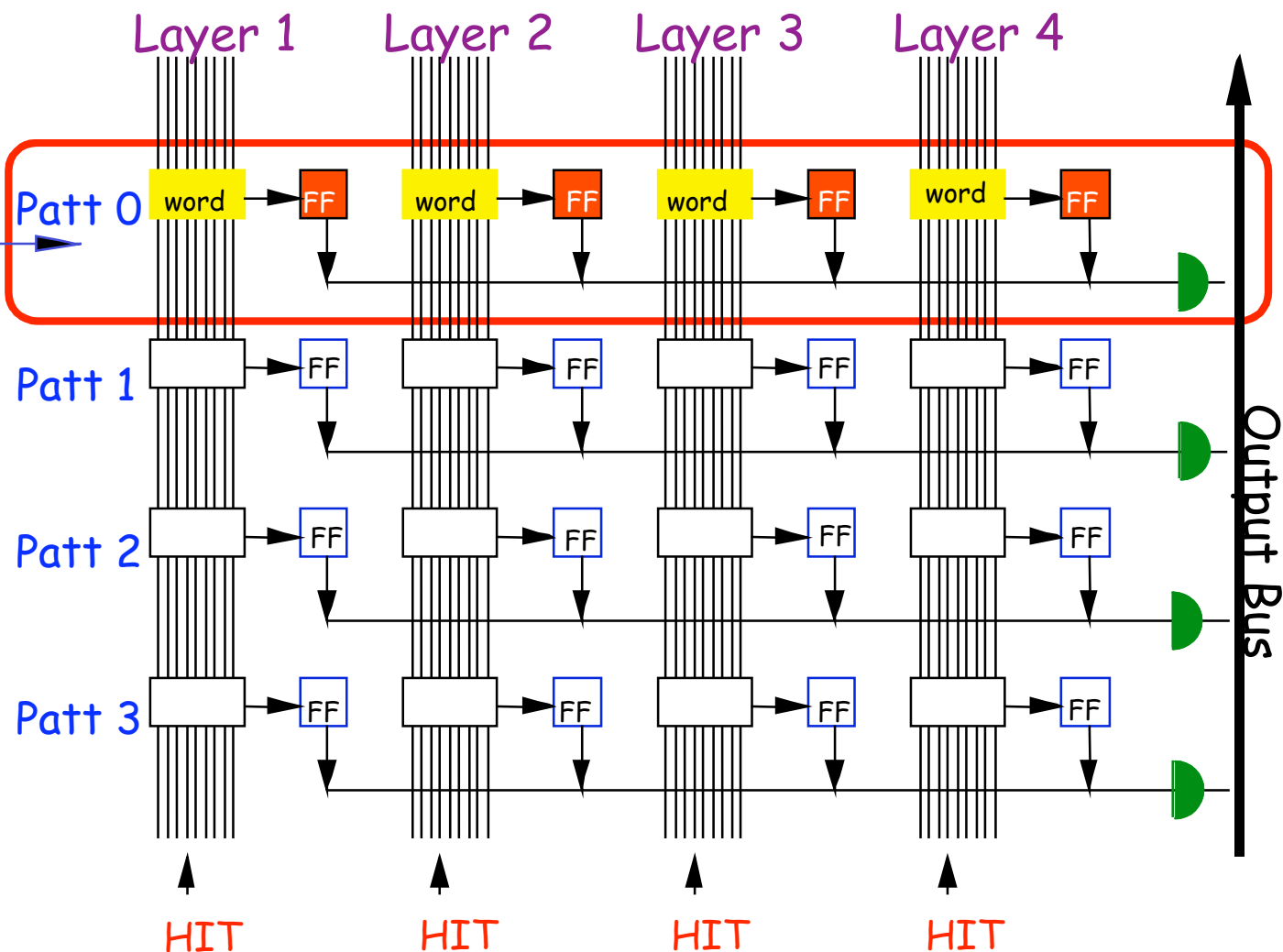
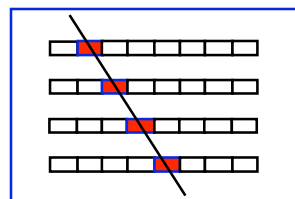
# AM: Associative Memory



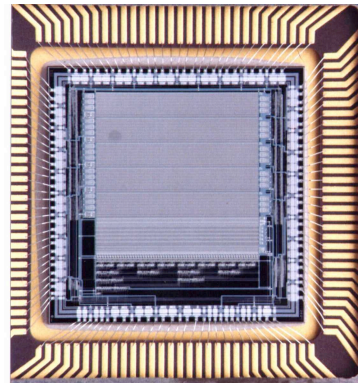
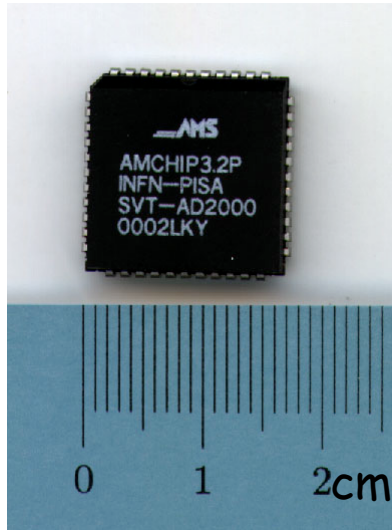
- Dedicated device: maximum **parallelism**
- Each pattern with **private comparator**
- Track search **during** detector **readout**

# AM chip working principle

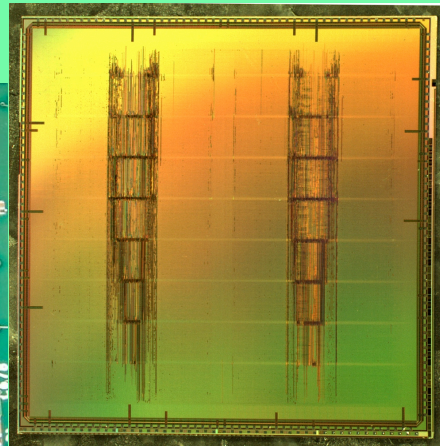
ONE PATTERN



# AMchip History



- Undoable with standard electronics (90's)
- ⇒ Full custom VLSI chip - 0.7 $\mu$ m (INFN-Pisa)
- 128 patterns, 6x12bit words each
- Working up to 40 MHz
- Single input bus



2.8 cm

1 cm

- Standard Cell design 2003-2004
- ⇒ Chip VLSI, technology 0.18 $\mu$ m UMC-IMEC (INFN Ferrara, INFN Pisa)
- 1cm<sup>2</sup> die size
- 5120 patterns, 6 words x 16bits each
- Tested up to 40MHz, Simulated up to 50MHz
- 6 input buses (x6 bandwidth)

# AMchip03 key features

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- Modular
  - Works with up to 6 detector layers (5120 patterns)
  - Or up to 12 detector layers (2560 patterns)
  - Up to 16bits per hit (65536 channels/layer: more chips --> more channels)
- High input Bandwidth:
  - 6 parallel input busses
  - Read input Hits at 6x40 MHz (x16bits=3.8Gbits)
  - Simulated up to 50MHz (design goal: 40MHz)
- Flexible:
  - Use array of AMchip03 for large pattern banks --> better resolution
  - Use different AMchip03 for different detector slices --> higher b/w
- General
  - Works for almost any detector; also mixed detectors
  - Accounts for misalignment
  - Works for inner trackers as well as muon trackers
  - Finds whole tracks, finds segments, combine segments (2D or 3D)

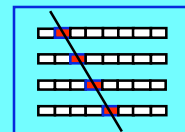
# AMchip03 Technical features

- Output data:

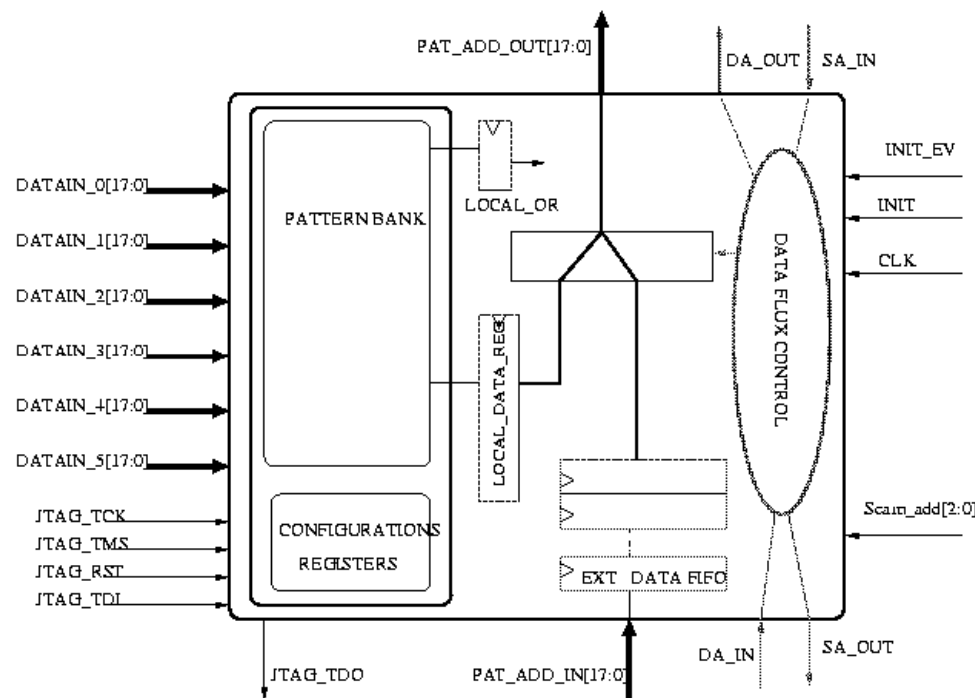
- Found pattern **addresses**

- **NEW!!** Fired **layer** bitmap (e.g. 110111 --> layer3 missing)

#1332



→ to LUT with  
track parameters



- IO pins: 164

- **JTAG interface**

- for configuration

- for loading patterns

- Build up **MEGA pattern** arrays

- Daisy chains

- Multiplexed

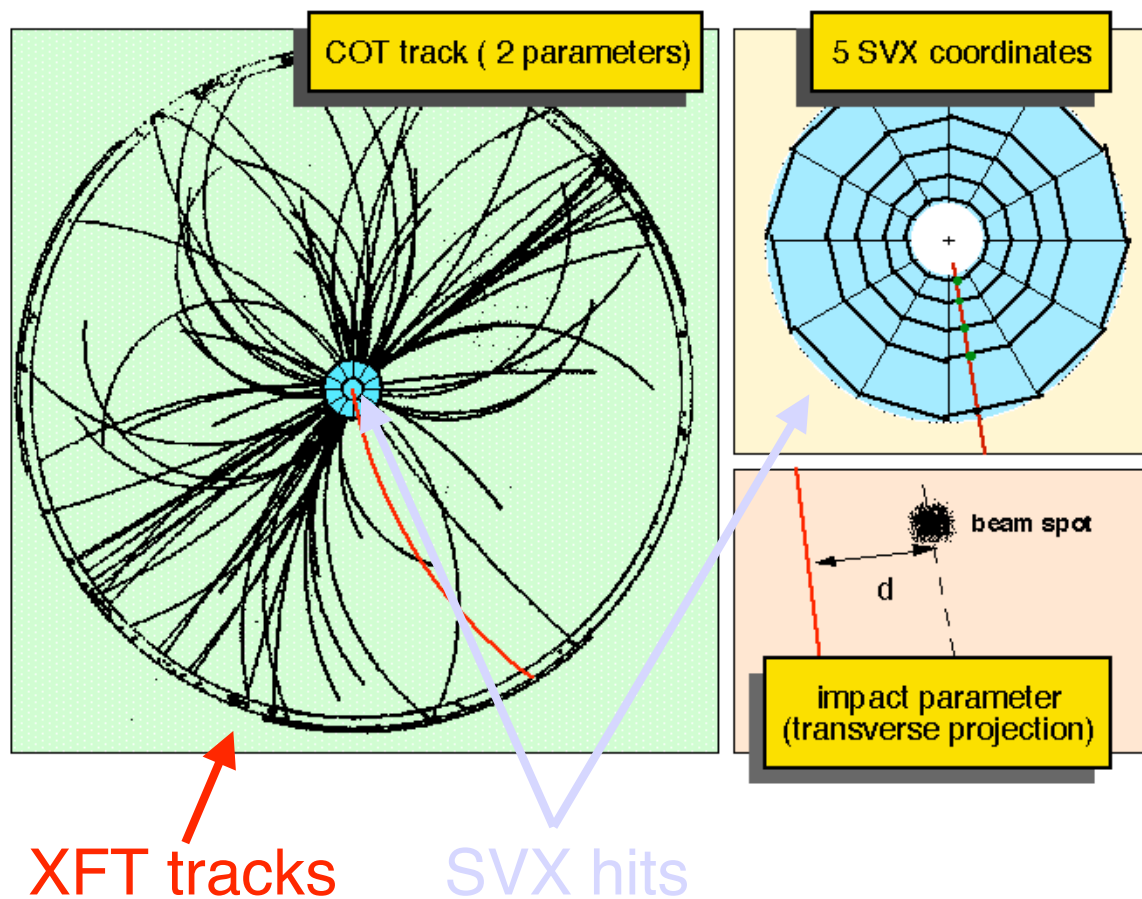
- Mixed

- Power consumption:

- IO (3.3V) 0.5W (upper limit)

- Core (1.8V) 1.2W (worst case)

# AMchip03 for the SVT upgrade

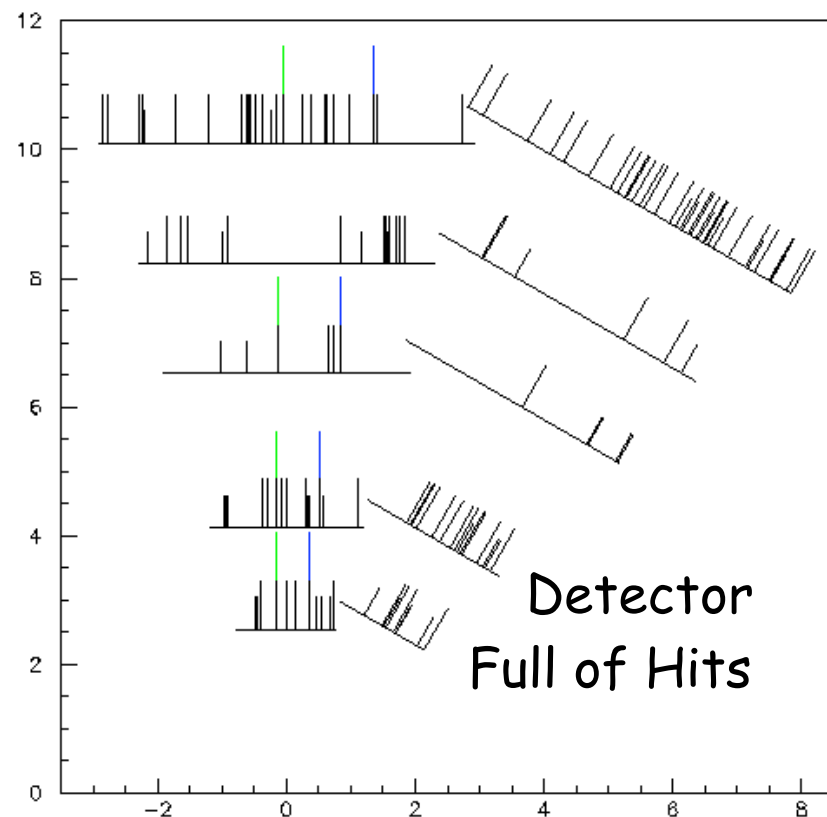
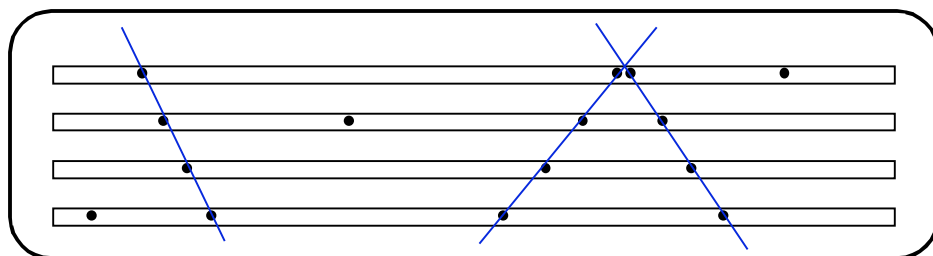
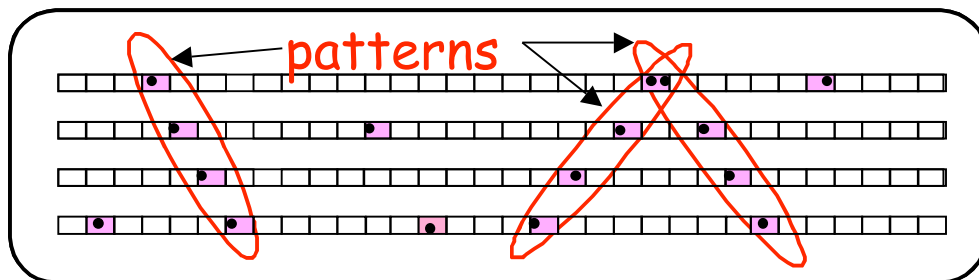


- Designed for the **SVT upgrade** --> part of CDF level-2 trigger
- Performs 2D **pattern recognition**
- Finds Tracks in the **CDF Silicon** detector
- Improves pattern-recognition **resolution** w.r.t previous AMchip

More info: [N14-117](#) - First Step of the Silicon Vertex Tracker upgrade at CDF

# AMchip03 application example

1. Find **higher resolution** tracks.  
Requires **more** patterns.  
Solve **most** of the pattern  
recognition



2. (optional) fit tracks inside  
roads. Thanks to 1<sup>st</sup> step  
it is much easier

# AMchip03 future applications

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- Currently used for SVT upgrade @ CDF
- Designed also for Fast-Track R&D: whole detector LVL2 tracking @ LHC  
[IEEE Trans. Nucl. Sci. 51, 391 (2004):  
Hadron Collider Triggers with Offline-Quality Tracking at Very High Event Rates]
- Considering LVL1 applications (many ideas here):
  - @  $e^+ e^-$  colliders
    - ☞ Could use current device
  - @  $p p$  colliders
    - ☞ Need faster clock frequency
    - ☞ Place AMchip processor on detector itself
      - Minimize data volume: extract only candidate tracks

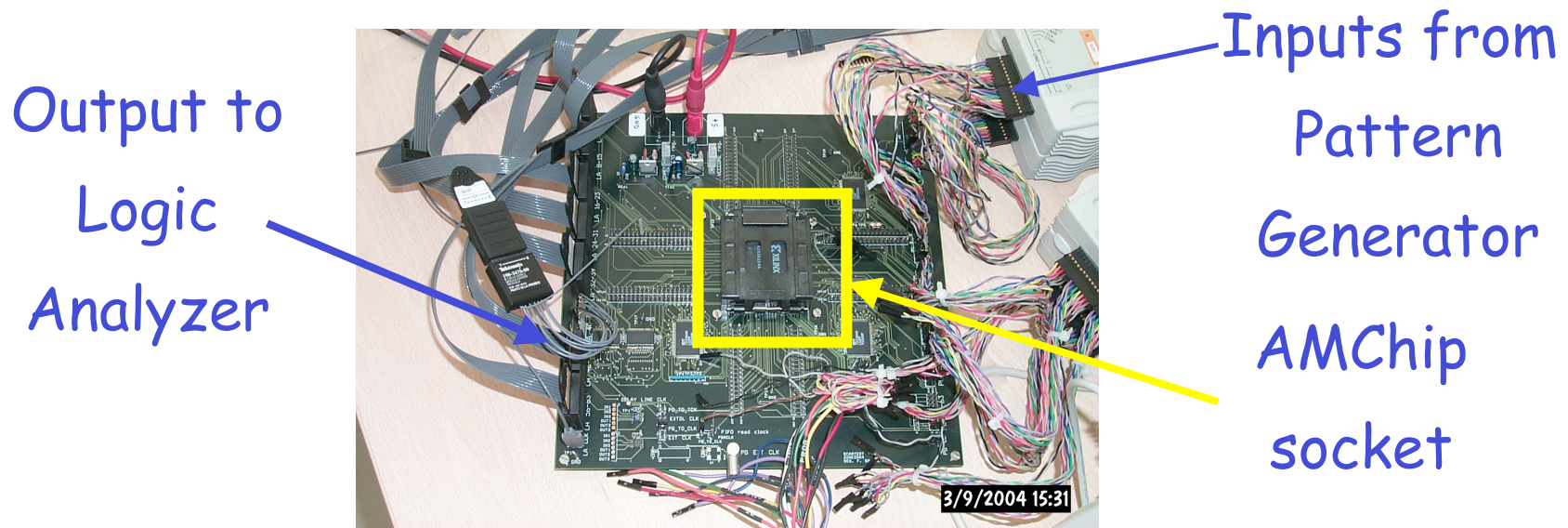


## Testing AMchip03 prototypes

116 prototype chips on September 2004

MPW run – **low yield 37%**

Characterization of failures: mostly single defect



3000 production chips on April 2005 **good yield 70%**

private masks → better process parameter tuning

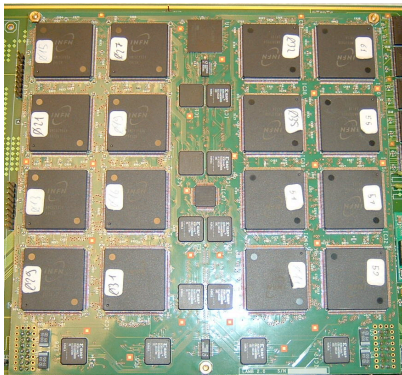
production testing → outsourcing **Microtest**

# AMchip03 Testing & Installation



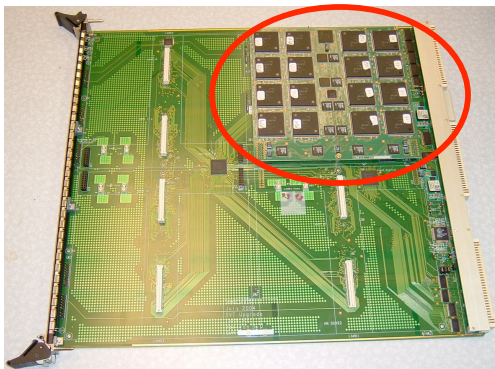
Developing the PCB with FPGAs  
(2 patterns instead of 5120)

Within 2 years  
of funding!!!



Ready for solder and test with  
ASIC just after prototyping.  
Up to 32 chip/board (2 sides)

July 21 2005:  
first AMchips  
Installed



9U VME board  
Up to 4 daughters  
Up to 128 AMchip03  
384 chips installed so far



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# Conclusions

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- We have developed a 5120-pattern AMchip03 processor for the SVT upgrade
- Take advantage of latest Silicon technology
  - Write specs to installation within 2 years!!
- It is powerful, general and flexible
- We are looking forward to share this technology
  - The AMchip03 processor can be reused saving development time
  - The very same device can be applied at other experiments
  - We are considering LVL1 applications

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